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The PCI Express Bus

Introduction

In the early 1990s, the PCI bus revolutionized I/O bus technology by replacing the numerous amounts of interface technology with its wider bandwidth, easy compatibility, and relatively high speeds [1]. The PCI bus allows for clock rates from 33 MHz to 512 MHz with the standard being 33 MHz in many systems [1]. Processor and clock speeds have been improving since the technology was first introduced producing a bottleneck on the latency of data transfer. The PCI Express (PCIe) bus proves to be on the forefront in replacing the widely used PCI due to its increased capabilities, allowing clock rates from 2.5 GHz to 10 GHz for each serial line [1]. This paper reviews the use of PCI Express bus technology in desktops, laptops, and servers.

PCI Express Technology Compared to Legacy PCI Technology

The PCI Express utilizes a layered architecture that consists of a physical layer, data link layer, and transaction layer [2]. The physical layer includes a high speed serial line, which is used to send PCI signals [3]. Since the PCI signals are not being altered, no changes in the software is needed meaning the PCIe interface is backwards compatible with PCI products [3]. The architecture allows for the bandwidth to a device to be increased by sending groups of serial lines to the device. There is a linear increase in bandwidth with number of lines grouped together [4]. This was not the case with PCI with its smaller, nonlinear increase with the number of lines grouped together. The PCI shared its total bandwidth of up to 512 MHz with all of its lines, but due to the serial lines going out, the PCIe has a bandwidth of up to 10 GHz for each line. The PCIe has more bandwidth per pin, so less pins are needed which decreases the overall physical size of the PCIe [4].

PCI Express Buses in Commercial Computers

Due to the improvements in PCIe technology compared to legacy technology, it has slowly been taking over in many components in commercially sold desktops and laptops, replacing the older AGP and PCI technologies [5]. Internal graphics cards, external graphics cards, and storage devices are the main adopters of PCIe [5]. GPUs were the first components to adopt the PCIe, and by 2013, PCIe became the standard interface for graphics cards on all new systems, which replaced the previous standard of AGP [5]. Many chipsets began adopting the technology, with Intel releasing their P35 Express chipset that utilizes PCIe connectors and buses [6]. External GPUs, which have the ability to allow a computer to operate faster by simply connecting the device to the computer, have also adopted the PCIe technology and all use this interconnect.

The PC Card slot included in many computers previously has been taken over by the ExpressCard slot, which uses the PCIe technology [7]. The ExpressCard/34 and ExpressCard/54 offer more bandwidth than the legacy PC Card with a maximum throughput of 2.5 Gbit/s due to

PCIe compared to 1.04 Gbit/s maximum due to PCI [7]. Most Dell, ASUS, Sony, Panasonic, Gateway, and many other companies have all included the ExpressCard slot in the design of their laptops [7].

PCIe technology has also been implemented in most high-end storage devices; the most common being solid-state drives (SSDs). The Dell PowerEdge Express Flash NVMe “Mixed Use” PCIe SSD is intended for a server system comprised of SSDs that are all connected by PCIe interface [8]. This interface technology plays a key role in big data storage and transfer within the server system. With a minimum of two-fold increase in bandwidth from the PCI to PCIe technology, it makes sense why most systems adopt the technology.

As all these components are adopting the technology which can be seen on a system level on processor boards. Some military systems are using processor boards with PCIe buses for the microprocessor, flash/RAM, and logic units to become more state-of-the-art [9].

Future

The future is looking bright for the PCI Express technology due to its architecture. The multilayer design allows for the physical bus to continually be improved with technology while the other layers do not need much improvements. The current PCIe 4.0 technology has nominal 2 GB/s bandwidth per lane and PCI-SIG (the company who manufactures and makes specifications for the PCIe) has already declared their intentions for PCIe 5.0 by 2019 with an expected nominal 4 GB/s bandwidth per lane [10]. As technology improves, so will the PCIe until it reaches it limit of around 10 GB/s, which is the maximum a signal can do in copper [3]. As the PCIe keeps taking over, it will monopolize the bus industry so most interfaces will be PCIe. Transfer latency in systems is one of the many factors in improving system speed and performance. Future improvements on the architecture and physical layer of the PCIe will be supplemental in producing the fastest systems to come.

References

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