# State of the Art Analog to Digital Converter Technology

## Introduction

Analog to Digital Converters (ADCs) are an integral component of almost all electronic application fields such as sensing technology, communication systems, and computers [1]. Today's technology advancements, more specifically the Internet of Things, have given rise to stringent requirements that require the use of ADCs. Because of this, there has been fierce industry competition and high research interest to find the most optimal solution to accommodate those requirements.

Analog to digital conversion is accomplished through multiple architectures, each yielding different parameters. Therefore, based on those parameters, each ADC architecture is best suited for a specific set of applications [2], [3]. This paper is a review of the latest ADC Technology; it particularly examines resolution, speed, size, noise, and power consumption in the context of various applications.

## Analog to Digital Converters Performance Parameters

**Resolution:** The range voltage represents the size of the range of possible input analog voltages. It is defined as $\mathrm{V_R} = V_{max} - V_{min}$. N is the number of bits of an ADC. The resolution of the ADC $\Delta\mathrm{V}$ is $\Delta\mathrm{V} = \frac{V_r}{2^N}$ [4].

**Speed:** Speed describes how many samples (digital words) are given by the ADC per second. The unit for speed is SPS (Samples per Second).

**SNR/ENOB:** SNR describes the ratio of the signal level to the introduced noise level [5]. Effective Number of Bits (ENOB) describes the number of bits factoring the noise. Sources of noise include the Aperture Noise (introduced by circuit clock) and Thermal Noise [1].

## Analog to Digital Converters Architectures

There are various ADC architectures with multiple performance metrics and targeted applications. The most commonly used architectures include Flash, Pipeline, Successive Approximation Registers, and Sigma-Delta [2], [6], [7]. This section will give a brief overview of those commonly used ADC architectures and provide the performance parameters of state-of-the-art ADCs available in the market.

### Flash ADCs

An N bit Flash ADC uses $2^{\mathrm{N}}$ equal resistors in series to divide a reference voltage in $\Delta\mathrm{V}$ steps and $2^{\mathrm{N}} - 1$ comparators to compare the input signal to each reference voltage step. A voltage high or a voltage low serves as the output of each comparator. The series of highs and lows is encoded to output a digital word [4], [6], [7], [8]. Because a Flash ADC requires a large number of components, it occupies large space and is expensive. Furthermore, as the number of bits is increased, parasitic capacitance is introduced to the ADC providing it with a high pass filter characteristic. On the other hand, because of its parallel nature, the Flash ADC has the highest speed of all ADC architectures. Another advantage is that it does not require a clock which is an added noise source [1], [6], [8].

Flash ADCs are used in high frequency applications such as communication and defense [2]. Analog Devices' Flash ADC HMCAD5831LP9BE has a speed of 26 GSPS but has a 3 bit resolution, consumes 4.2 W, and costs about $3,000 [9], [10]. Texas Instruments' Flash ADC12J4000 has a speed of 4 GSPS with 12 bits resolution. It consumes 2 W and costs about $2,229 [10]. The minimum ADC12J4000 SNR varies from 49 dB to 53 dB depending on operation mode [11].

### Pipeline ADCs

The Pipeline ADC compares the input voltage to a set of reference values similar to a Flash ADC. However, a Pipeline ADC compares the values in series rather than in parallel. Therefore, the reference voltages are dependent on the input voltage rather than a predetermined voltage value. The series architecture of the Pipeline ADC requires it to have an S&H (sample and hold) mechanism. To satisfy this requirement, a clock is needed which introduces a noise source [6].

While a Pipeline ADC requires more devices per stage than a Flash ADC, a Pipeline ADC adds 3 bits of resolution per stage. The speed of Pipeline ADCs is typically few hundreds of MSPS slower than that of Flash ADCs [12]. On the other hand, due to the lower number of devices needed to get to a specific number of bits, a Pipeline ADC consumes less power, occupies less space, and is cheaper.

In general, low cost, reduced size, and higher resolution make the Pipeline ADC the most popular option for high speed applications [2], [12]. Such applications include imaging, defense, video, and communication. Texas Instruments' dual channel Pipeline ADC ADC32RF45 costs $1800 [10]. It has 14 bits of resolution, a speed of 3GSPS, a power dissipation of 3.2 W and an SNR of 60.9 dB [13].

### Successive Approximation Register (SAR) ADCs

A SAR ADC samples the input voltage with an S&H mechanism. Using a single comparator, it compares the input voltage to a reference voltage. It makes use of a register to record the output digital word which represents the input voltage. This recorded word is used to determine the next reference voltage. A higher resolution is reached by changing the reference voltage over multiple clock cycles. Essentially, the input voltage is found through a binary search algorithm. This process requires a Digital to Analog Converter (DAC) [4], [6], [7], [14].

SARs require fewer devices than Pipeline ADCs and Flash ADCs. Therefore, SARs are cheaper, more compact and consume less power. However, SARs are slower than Pipeline and Flash ADCs [6].

Analog Devices' SAR ADADC80-12 has a speed of 40 MSPS, a power dissipation of 0.8 W, a 12 bit resolution [15], and costs $295 [10]. A SAR ADC is used for low frequency applications such as temperature sensors [2].

### Sigma Delta ($\Delta\Sigma$) ADCs

A Sigma Delta ADC is a closed negative feedback loop. The feedback is subtracted from the input voltage. The integrator adds the sum to a value stored from the previous integration. If the non-inverting input of the op-amp is greater than zero a logic high is output, otherwise a logic low is output. Over multiple cycles, this sum will equal zero due to the negative feedback. The output of this feedback loop is a digital word that is used to determine the input voltage [6], [7], [16]. Because of this architecture that requires multiple cycles of feedback to accurately determine the input voltage, the Delta Sigma is generally slower than the SAR ADC.

The Delta Sigma ADC stands out for having high resolution and SNR with low power dissipation. It oversamples the input voltage (sample rate is much higher than nyquist rate). A Delta Sigma ADC is generally more expensive than an SAR ADC. It is, however, cheaper than the Flash and Pipeline ADCs [2], [7], [16].

Analog Devices' $\Delta\Sigma$ ADC AD9267BCPZ has a resolution of 16 bits with a speed of 600 MSPS, SNR of 83 dB, power dissipation of 0.5 W [18], and cost of $63 [10]. A Delta Sigma is used for high precision, low frequency applications.

### Going Beyond State of the Art

Multiple ADCs can be used simultaneously to convert the same signal. Averaging of those ADCs is used to increase the SNR by 3.01 dB for every 2 ADCs added. In addition, with proper phasing, multiple ADCs can be combined to produce a higher speed Analog to Digital Converter. Phasing multiple ADCs to increase speed is called Time Interleaving [5].

## References


[1] B. Le, T. Rondeau, J. Reed, and C. Bostian. (2005, Nov). Analog-to-Digital Converters. IEEE Signal Processing Magazine, vol. 22, no. 6, [Web]. 69-77. Available: http://ieeexplore.ieee.org.prx.library.gatech.edu/document/1550190/

[2] "Choose the right A/D converter for your application," Choose the right A/D converter for your application. Texas Instruments. Available: https://www.ti.com/europe/downloads/Choose%20the%20right%20data%20converter%20for%20your%20application.pdf

[3] "What is an Analog to Digital Converter?," What is an analog to digital converter, adc, audio analog, tv - Future Electronics. [Online]. Available: http://www.futureelectronics.com/en/data-converters/analog-to-digital-converters.aspx. [Accessed: 23-Oct-2017].

[4] M. Leach, T. Brewer, and A. Robinson, "Analog to Digital and Digital to Analog Conversion Systems," in *Experiments in Analog Electronic Circuits*, 1st ed. Dubuque, IA: Kendall Hunt, 2013, ch. 13, sec. 1-5, pp. 201–218.

[5] R. Reeder, M. Looney, and J. Hand. (2015, May). Pushing the State of the Art with Multichannel A/D Converters. Analog Dialogue [Web]. 39(05). Available: http://www.analog.com/media/cn/analog-dialogue/volume-39/number-2/articles/multichannel-a-d-converters_cn.pdf

[6] H. Gonçalves, "Analog-Digital Converters," *onmyphd*.com [Online]. Available: http://www.onmyphd.com/?p=analog.digital.converter#h3_sigmadelta. [Accessed: 23-Oct-2017].

[7] J. Pytel, "ADC," YouTube, 15-Jul-2010. [Online]. Available: https://www.youtube.com/watch?v=7X53_QCXbjk&t=1899s. [Accessed: 23-Oct-2017].

[8] T. R. Kuphaldt, "Flash ADC," in *Lessons in Electric Circuits*, 4th ed. 2007, ch. 13. Available: https://www.allaboutcircuits.com/textbook/digital/chpt-13/flash-adc/

[9] Analog Devices, "3-BIT 26 GSPS ANALOG-TO-DIGITAL CONVERTER W/ OVERRANGE, INHIBIT, AND 1:2 DEMUX," HMCAD5831LP9BE datasheet, Feb. 2017.

[10] "Mouser Electronics - Electronic Components Distributor*," Mouser Electronics - Electronic Components Distributor*. [Online]. Available: https://www.mouser.com/. [Accessed: 23-Oct-2017].

[11] Texas Instruments, "12-Bit, 4-GSPS ADC With Integrated DDC," ADC12J4000 datasheet, Jan. 2014 [Revised Oct. 2017].

[12] "Understanding Pipelined ADCs," *Understanding Pipelined ADCs - Tutorial - Maxim*. [Online]. Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023. [Accessed: 23-Oct-2017].

[13] Texas Instruments, "Dual-Channel, 14-Bit, 3.0-GSPS, Analog-to-Digital Converter," ADC32RF45 datasheet, May. 2016 [Revised Dec. 2016].

[14] R. Perry, "24-Bit 2Msps SAR ADC with Digital Filter Simplifies Your System," YouTube, 29-Feb-2016. [Online]. Available: https://www.youtube.com/watch?v=Cp2qSLKquVM. [Accessed: 23-Oct-2017].

[15] Analog Devices, "12-Bit Successive-Approximation Integrated Circuit ADC," ADADC80 datasheet, Feb. 2017.

[16] "Sigma-Delta ADC Tutorial," Sigma-Delta ADC Tutorial | Design Center | Analog Devices. [Online]. Available: http://www.analog.com/en/design-center/interactive-design-tools/sigma-delta-adc-tutorial.html. [Accessed: 23-Oct-2017].

[17] T. Xingyuan, J. Chen, Z. Zhu and Y. Yintang. (2010). A high performance 90 nm CMOS SAR ADC with hybrid architecture. Journal of Semiconductors. 31. 015002. 10.1088/1674-4926/31/1/015002. Available: https://www.researchgate.net/figure/231126079_fig1_Fig-1-Typical-SAR-ADC-architecture. 2017.

[18] Analog Devices, “10 MHz Bandwidth, 640 MSPS Dual Continuous Time Sigma-Delta Modulator,” AD9267 datasheet, Sept. 2017.